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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/957,415	09/20/2001	Scott Thomas Elliott	RPS9 2001 0044	3264

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SAWYER LAW GROUP LLP
PO BOX 51418
PALO ALTO, CA 94303

EXAMINER	
CHAI, LONGBIT	

ART UNIT	PAPER NUMBER
2131	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/957,415	ELLIOTT ET AL.	
	Examiner	Art Unit	
	Longbit Chai	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Original application contained claims 1 – 22. Claims 5 and 13 have been amended in an amendment filed on 9/5/2006. The amendment filed have been entered and made of record. Presently, pending claims are 1 – 22.

Response to Arguments

2. Applicant's arguments with respect to instant claims have been fully considered but are not persuasive.

3. This is the 2nd Final action that allows the entry of Applicant amendments filed 9/5/2006. However, the *35 USC § 112*, 2nd paragraph rejection still holds for claims 5 and 13 because an encrypting key, as amended, is indefinite and unclear since each of the hardware key, a platform key and a user key, as recited in the claim, is also, by nature, an encrypting key. Refer to the following Office action as set forth below.

4. As per claim 1, 7 and 16, Applicant asserts that there is apparently no separate, dedicated embedded security processor on a system board along with an additional processor and consequently, Kern fails to teach or suggest the use of the recited embedded security processor (Remarks: Page 9 Last Para). Examiner respectfully disagrees because (a) Applicant's argument has no merit since the alleged limitation has not been recited into the claim that there is a separate and additional embedded security processor, as presented in the argument; instead, the submitted claim limitation merely recites "utilization with an embedded security chip of the computer system" and

therefore Examiner notes, first, the chip is not necessary a processor and secondly, a microprocessor itself that performs security functions is indeed an embedded security processor. (b) Kern discloses the security module comprises a hardware module such as microprocessor, ASIC and etc (Kern: Column 6 Line 49 – 51) and as such Kern does teach embedded security processor and chip and as such applicant's arguments are respectfully traversed.

5. As per claim 1, 7 and 16, Applicant asserts that Kern fails to turn up the term "tag" associated with the key. Examiner respectfully disagrees because Kern teaches the default tag data value (for example: FFFF) indicates no security and a security key is not required to be presented (Kern: Column 11 Line 8 – 10) and as such Kern does teach embedded security processor and chip and as such applicant's arguments are respectfully traversed.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 5 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 and 13 are indefinite because the claim language "the four levels further comprise a hardware key pair level, a platform key pair level, an encrypting key pair level, and a user key pair level" is not clear what exactly it means. Specifically

speaking, an encrypting key, as recited, is indefinite and unclear since each of the hardware key, a platform key and a user key, as recited in the claim, is also, by nature, an encrypting key.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraph of 35 U.S.C. 102 that forms the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1 – 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Kern et al. (U.S. Patent 6,446,209).

As per claim 1, 7 and 16, Kern teaches a method for control of key pair usage in a computer system, the method comprising:

creating key pair material for utilization with an embedded security chip of the computer system (Kern: Column 6 Line 56 – 63, Column 6 Line 47 – 51 and Column 11 Line 55 & Figure 1 / Element 106/122/124: a "reference location" per storage use map in a microprocessor-based security module is residing on a memory chip associated with a microprocessor (Figure 1 / Element 122) and a storage element (Figure 1, Element 108)),

the key pair material including tag data, the tag data indicating whether the key pair material is bound to a specific computer based on the tag data without indicating an identity of the embedded security chip or the computer system (Kern: Column 11 Line 8 – 10: the default tag data value (for example: FFFF) indicates no security (or non-binding)); and

determining whether the key pair material is bound to a specific computer based on the tag data (Kern: Column 11 Line 8 – 10).

As per claim 2, 9 and 17, Kern teaches comprising a bit to indicate whether binding is required for the key pair material (Kern: Column 10 Line 66 – Column 11 Line 10: BIT-1 || BIT-0: "X||0": non-binding // "0||1": RD/WR Protect // "1||1" WR Protect and therefore 1-bit, i.e. BIT-0, is sufficient for this purpose).

As per claim 3 and 11, Kern teaches creating key pair material further comprises creating key pair material of different levels (Kern: Column 6 Line 56 – 63, Column 7 Line 23 – 26, Column 15 Line 13 – 19 and Column 16 Line 32 – 36).

As per claim 4, 5, 12 and 13, Kern teaches the four levels further comprise a hardware key pair level, a platform key pair level, an encrypting key pair level, and a user key pair level (Kern: Column 6 Line 56 – 63, Column 7 Line 23 – 26 and Column 15 Line 13 – 19 and Column 16 Line 32 – 36).

As per claim 6 and 14, Kern teaches tag data further comprises including a tag for indicating binding is required for the platform key pair level (Kern: Column 14 Line 44 – 48, Column 15 Line 13 – 19 and Column 16 Line 32 – 36: the security key and operation parameters provided at the time of manufacturing (or by system administrator) is qualified as a "platform key").

As per claim 8, Kern teaches comprising means for security setup to provide an interface on the computer system for administration of the security processor, including providing the tag data (Kern: Column 14 Line 44 – 48, Column 15 Line 13 – 19 and Column 16 Line 32 – 36: the security key and operation parameters provided at the time of manufacturing (or by system administrator) is qualified as a "platform key").

As per claim 10, Kern teaches the security processor includes memory for storing the key pair material (Kern: Column 6 Line 56 – 63, Column 6 Line 47 – 51 and Column 11 Line 55 & Figure 1 / Element 106/122/124: a "reference location" per storage use map in a microprocessor-based security module is residing on a memory chip associated with a microprocessor (Figure 1 / Element 122) and a storage element (Figure 1, Element 108)).

As per claim 15, Kern teaches the key pair material further comprises a tag to indicate binding is not required for the user key pair level (Kern: Column 15 Line 13 – 19

and Column 16 Line 32 – 36: the security key provided by the user input is qualified as user key pair).

As per claim 18, Kern teaches utilizing the reset tag bit with a user key pair level in the hierarchical structure to allow user key pairs to be verified securely on more than one computer system (Kern: Figure 5 / Element 506 / 508, Column 15 Line 52 – 55 and Column 11 Line 8 – 10).

As per claim 19, Kern teaches utilizing the set tag bit with a platform key pair level in the hierarchical structure to allow a platform key pair to be verified only on a computer system where binding with the embedded security chip is established (Kern: Column 15 Line 13 – 19 and Column 16 Line 32 – 36 and Column 11 Line 8 – 10).

As per claim 20, 21 and 22, Kern teaches the hierarchical structure is organized such that key pair material for a portion of each of at least two levels of the hierarchical structure are not bound (Kern: Column 15 Line 13 – 19 and Column 16 Line 32 – 36 and Figure 5 / Element 506 / 508 and Column 15 Line 52 – 55).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Longbit Chai whose telephone number is 571-272-3788. The examiner can normally be reached on Monday-Friday 8:00am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R. Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Longbit Chai
Examiner
Art Unit 2131

LBC

CHRISTOPHER REVAK
PRIMARY EXAMINER

9/14/06